We claim:

1. A method of preparing a pre-formed integrated circuit chip for encapsulation in an electronic package, comprising the steps of:

forming an interconnect assembly separately from said pre-formed integrated circuit chip;

forming a plurality of conductive bumps connected to the terminals of the integrated circuit chip;

bonding said interconnect assembly to said prepared integrated circuit chip; and

passivating said bonded interconnect assembly and said prepared integrated circuit chip into an integral structure to provide said electronic package.

2. The method of claim 1 wherein said step of forming an interconnect assembly comprises forming said interconnect assembly on a releasable substrate.

3. The method of claim 1 wherein said step of forming an interconnect assembly comprises forming at least one test pad in an interconnect layer, which at least one test pad can be accessed and electrically connected on opposing sides of said test pad.

4. The method of claim 3 wherein said step of forming at least one test pad forms a test pad having gold on opposing sides of said test pad and sandwiched therebetween a conductive field metal.

5. The method of claim 3 wherein said step of forming an interconnect assembly comprises forming at least one test pad in a plurality of stacked interconnect layers, each of which at least one test pad in each interconnect layer can be accessed and electrically connected on opposing sides of said test pad.

6. The method of claim 5 wherein said step of forming at least one test pad in a plurality of stacked interconnect layers forms at least one test pad in each layer having gold on opposing sides of said test pad and sandwiched therebetween a conductive field metal.

7. The method of claim 1 where said step of forming a plurality of conductive bumps connected to the terminals of the integrated circuit chip form a metallic bump making connection to a terminal on said integrated circuit chip and a solder layer disposed on said metallic bump.

8. The method of claim 7 wherein said step of forming an interconnect assembly comprises forming at least one test pad in an interconnect layer, which at least one test pad can be accessed and electrically connected on opposing sides of

said test pad, and wherein said step of bonding said interconnect assembly to said prepared integrated circuit chip flip bonds said solder layer onto one side of said test pad.

9. The method of claim 1 where said step of passivating said bonded interconnect assembly and said prepared integrated circuit chip into an integral structure to provide said electronic package comprises underfilling said prepared integrated circuit chip with an insulating material to remove all voids between said prepared integrated circuit chip and said interconnect assembly.

10. The method of claim 1 where said step of passivating said bonded interconnect assembly and said prepared integrated circuit chip into an integral structure to provide said electronic package comprises potting said interconnect assembly and said prepared integrated circuit chip into an integral package.

11. The method of claim 9 where said step of passivating said bonded interconnect assembly and said prepared integrated circuit chip into an integral structure to provide said electronic package comprises potting said interconnect assembly and said prepared integrated circuit chip into an integral package.

12. The method of claim 10 further comprising the step thinning said prepared integrated circuit chip.

13. The method of claim 10 further comprising the step of accessing said prepared integrated circuit chip through electrical connection to said at least one test pad through a surface thereof opposing said surface of said test pad contacting a terminal of said prepared integrated circuit chip to test said prepared integrated circuit chip.

14. The method of claim 10 wherein a plurality of interconnect assembly and prepared integrated circuit chips are bonded together to form a corresponding plurality of electronic packages and further comprising the step of releasing said plurality of electronic packages from each other.

15. The method of claim 1 wherein a plurality of interconnect assembly and prepared integrated circuit chips are bonded together to form a corresponding plurality of electronic packages and further comprising the step of testing said interconnect assembly and bonding a tested interconnect assembly in said step of bonding said interconnect assembly to said prepared integrated circuit chip only if said interconnect assembly tested good.

16. The method of claim 15 where said step of forming said plurality of interconnect assemblies comprises forming said interconnect assemblies simultaneously in a wafer and where said plurality of prepared integrated circuit chips are individually bump bonded to successfully tested ones of said interconnect assemblies.

17. An electronic package comprising:

a pre-formed integrated circuit chip;

an interconnect assembly separately from said pre-formed integrated circuit chip;

a plurality of conductive bumps connected to the terminals of the integrated circuit chip, said interconnect assembly bonded to said prepared integrated circuit chip; and

a passivating layer disposed about said interconnect assembly and said prepared integrated circuit chip after said interconnect assembly and said prepared integrated circuit chip have been bonded together thereby forming into an integral structure.

18. The electronic package of claim 17 wherein said interconnect assembly comprises is formed on a releasable substrate.

19. The electronic package of claim 1 wherein said interconnect assembly comprises at least one test pad in an interconnect layer, which at least one test pad can be accessed and electrically connected on opposing sides of said test pad.

20. The electronic package of claim 19 wherein said at least one test pad forms a test pad has gold on opposing sides of said test pad and sandwiched therebetween a conductive field metal.

21. The electronic package of claim 19 wherein said interconnect assembly comprises a plurality of stacked interconnect layers and at least one test pad in said plurality of stacked interconnect layers, each of which at least one test pad in each interconnect layer can be accessed and electrically connected on opposing sides of said test pad.

22. The electronic package of claim 21 wherein said at least one test pad in said plurality of stacked interconnect layers forms at least one test pad in each layer having gold on opposing sides of said test pad and sandwiched therebetween a conductive field metal.

23. The electronic package of claim 17 where said plurality of conductive bumps are connected to terminals of the integrated circuit chip in order to make a connection to said terminals on said integrated circuit chip and further comprising a solder layer disposed on said conductive bump.

24. The electronic package of claim 23 wherein said interconnect assembly comprises at least one test pad in said interconnect layer, which at least one test pad can be accessed and electrically connected on opposing sides of said test pad, and wherein said interconnect assembly is bonded to said prepared integrated circuit chip by a flip bond to said solder layer onto one side of said test pad.

25. The electronic package of claim 17 where said passivating layer combines said interconnect assembly and said prepared integrated circuit chip into an integral structure and includes insulating material underfilling of said prepared integrated circuit chip to remove all voids between said prepared integrated circuit chip and said interconnect assembly.

26. The electronic package of claim 17 where said passivating layer combines said interconnect assembly and said prepared integrated circuit chip into an integral structure and is comprised of a potting material.

27. The electronic package of claim 25 where said passivating layer combines said interconnect assembly and said prepared integrated circuit chip into an integral structure and is comprised of a potting material.

28. The electronic package of claim 26 where said prepared integrated circuit chip is thinned after being potted.

29. The electronic package of claim 27 said prepared integrated circuit chip is accessed through electrical connection to said at least one test pad through a surface thereof opposing said surface of said test pad contacting a terminal of said prepared integrated circuit chip to test said prepared integrated circuit chip.

30. The electronic package of claim 27 wherein a plurality of interconnect assembly and prepared integrated circuit chips are bonded together to form a corresponding plurality of electronic packages which are later released from each other.

31. The electronic package of claim 17 wherein a plurality of interconnect assembly and prepared integrated circuit chips are bonded together to form a corresponding plurality of electronic packages in which said interconnect assemblies are tested and a tested interconnect assembly is bonded to said prepared integrated circuit chip only if said interconnect assembly tested good.

32. The electronic package of claim 31 where in said plurality of interconnect assemblies said interconnect assemblies are formed simultaneously in a wafer and where said plurality of prepared integrated circuit chips are individually bumped bonded to successfully tested ones of said interconnect assemblies.